AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-79 (Canceled)

80. (Previously Presented) A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving a removable memory storage device, comprising:

a programmable graphics processor;

a main processor that executes at least a portion of a videographics generating game program that includes instructions for displaying polygon-based 3D graphic objects and which communicates information relating to one or more polygon-based 3D graphic objects to said programmable graphics processor,

wherein the programmable graphics processor is contained within the removable memory storage device and is programmed to render at least one or more portions of said 3D polygon-based graphic objects for display on said display device.

81. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor is a coprocessor that is responsive to specific instructions used for rendering polygon-based 3D objects.

82. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor is a pipelined processor.

Claim 83 (canceled)

84. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor includes embedded RAM cache memory.

85. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor includes graphics geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

86. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

87. (Previously Presented) A home video game system as set forth in claim 86 wherein the multiplier performs multiply operations using at least 16-bit length operands.

88. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

89. (Previously Presented) A home video game system as in claim 80 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

90. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor is programmed to perform texture mapping operations.

91. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

92. (Previously Presented) A home video game system as in claim 80 having a set of instructions for programming the programmable graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

93. (Previously Presented) A home video game system as in claim 80 having a set of instructions for programming the programmable graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

94. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

95. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

96. (Previously Presented) A home video game system as in claim 80 wherein the programmable graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

97. (Previously Presented) A home video game system as in claim 80 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

98. (Previously Presented) A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing having an insertion port for receiving removable memory, comprising:

a game program processing unit for executing at least a portion of a videographics game program that includes instructions for displaying polygon-based 3D objects; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects from said game program processing unit, the programmable graphics processor programmed to process pixel data for rendering one or more portions of polygon-based 3D objects for display on said television type monitor display.

99. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor is a coprocessor that is responsive to specific instructions used for rendering polygon-based 3D objects.

100. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor is a pipelined processor.

101. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes a high speed multiplier circuit.

102. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes embedded RAM cache memory.

103. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes graphics geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

104. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes at least an Arithmetic Logic Unit and a plurality of registers for executing instructions for performing rotation and/or scaling of a polygon-based graphic object to be displayed.

105. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

106. (Previously Presented) A home video game system as set forth in claim 105 wherein the multiplier performs multiply operations using at least 16-bit length operands.

107. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

108. (Previously Presented) A home video game system as in claim 98 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

109. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor is programmed to perform texture mapping operations.

110. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

111. (Previously Presented) A home video game system as in claim 98 having a set of instructions for programming the programmable graphics processor unit for rendering 3D graphic objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

112. (Previously Presented) A home video game system as in claim 98 having a set of instructions for programming the programmable graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

113. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

114. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

115. (Previously Presented) A home video game system as in claim 98 wherein the programmable graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

116. (Previously Presented) A home video game system as in claim 98 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

117. (Previously Presented) A home video game system for use with a television type display device said system contained at least in part in a housing having an insertion port for receiving a removable memory storage device storing video game program instructions and/or data, comprising:

a game program processor; and

a graphics processor for rendering at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, said graphics processor including a programmable processor having embedded RAM cache memory.

118. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

119. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor is a pipelined processor.

120. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor includes a high speed multiplier circuit.

121. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor includes a plurality of data storage registers.

122. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor includes graphic geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

123. (Previously Presented) A home video game system as in claim 122 wherein the geometry transformation circuitry includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

124. (Previously Presented) A home video game system as set forth in claim 123 wherein the multiplier circuit performs multiply operations using at least 16-bit length operands.

125. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

126. (Previously Presented) A home video game system as in claim 117 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

127. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor is programmed to perform texture mapping operations.

128. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

129. (Previously Presented) A home video game system as in claim 117 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

130. (Previously Presented) A home video game system as in claim 117 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

131. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

132. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

133. (Previously Presented) A home video game system as in claim 117 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

134. (Previously Presented) A home video game system as in claim 117 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

135. (Previously Presented) A home video game system, for use with a television type monitor display device, said system having a housing and an insertion port in the housing for receiving removable program memory, comprising:

a game program processing unit for executing at least a portion of a videographics program that includes instructions for displaying polygon-based 3D graphic objects;

a video RAM for providing video frame data to a display device; and

a programmable graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygon-based 3D graphic objects, the graphics processor programmed to process pixel data for subsequent transfer to said video RAM corresponding to one or more portions of polygon-based objects to be displayed.

136. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

137. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor is a pipelined processor.

138. (Previously Presented) A home video game system as in claim 135 wherein the transfer of pixel data to video RAM is a direct memory access (DMA) type transfer.

139. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes a high speed multiplier circuit.

140. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes embedded RAM cache memory.

141. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

142. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

143. (Previously Presented) A home video game system as set forth in claim 142 wherein the multiplier performs multiply operations using at least 16-bit length operands.

144. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

145. (Previously Presented) A home video game system as in claim 135 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

146. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor is programmed to perform texture mapping operations.

147. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

148. (Previously Presented) A home video game system as in claim 135 having a set of instructions for programming the graphics processor unit for rendering 3D graphic objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

149. (Previously Presented) A home video game system as in claim 135 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

150. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

151. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

152. (Previously Presented) A home video game system as in claim 135 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

153. (Previously Presented) A home video game system as in claim 135 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

154. (Previously Presented) A home video game system for use with a television type monitor display device comprising:

a housing including an insertion port that receives a removable memory storing video game program data/instructions;

a game program processor that executes at least a portion of a videographics game program that includes instructions for polygon-based 3D objects; and

a graphics processor that renders at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, the graphics processor including at least an Arithmetic Logic Unit and graphics geometry transformation circuitry for accelerating polygon-based 3D graphics transformation operations.

155. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

156. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor is a pipelined processor.

157. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor is a programmable pipelined processor.

158. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor includes embedded RAM cache memory.

159. (Previously Presented) A home video game system as in claim 154 wherein the graphics geometry transformation circuitry includes a high speed multiplier for performing computations for performing rotation and/or scaling of a polygon-based 3D graphic object or portions of the object to be displayed.

160. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

161. (Previously Presented) A home video game system as set forth in claim 160 wherein the multiplier performs multiply operations using at least 16-bit length operands.

162. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

163. (Previously Presented) A home video game system as in claim 154 wherein two or more polygon-based graphic objects are displayed simultaneously.

164. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor is programmed to perform texture mapping operations.

165. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

166. (Previously Presented) A home video game system as in claim 154 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

167. (Previously Presented) A home video game system as in claim 154 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

168. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

169. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

170. (Previously Presented) A home video game system as in claim 154 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

171. (Previously Presented) A home video game system as in claim 170 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

172. (Previously Presented) A home video game system for use with a television type monitor display device, said system having a housing and an insertion port in the housing for receiving removable memory and including a game program processor and a graphics processor for rendering at least one or more portions of a polygon-based 3D graphic object for displaying on the display device, the graphics processor comprising:

a programmable pipelined processor having an Arithmetic Logic Unit;

a multiplier unit;

a cache RAM; and

a plurality of registers;

wherein the graphics processor performs at least rotation and/or scaling operations on said polygon-based 3D graphic objects.

173. (Previously Presented) A home video game system as in claim 172 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

174. (Previously Presented) A home video game system as in claim 172 wherein the graphics processor includes hardware geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

175. (Previously Presented) A home video game system as set forth in claim 172 wherein the multiplier performs multiply operations using at least 16-bit length operands.

176. (Previously Presented) A home video game system as in claim 172 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

177. (Previously Presented) A home video game system as in claim 172 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

178. (Previously Presented) A home video game system as in claim 172 wherein the graphics processor is programmed to perform texture mapping operations.

179. (Previously Presented) A home video game system as in claim 172 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

180. (Previously Presented) A home video game system as in claim 172 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

181. (Previously Presented) A home video game system as in claim 172 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

182. (Previously Presented) A home video game system as in claim 172 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

183. (Previously Presented) A home video game system as in claim 172 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

184. (Previously Presented) A home video game system as in claim 172 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

185. (Previously Presented) A home video game system as in claim 184 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.

186. (Previously Presented) In a home video game system having a housing and an insertion port in the housing for receiving a removable memory for storing a video game program, said system including a game program processor for executing at least a portion of a video graphics program that includes instructions for displaying polygon-based 3D objects, a programmable graphics processor and a video RAM for providing video frame data to a television type monitor display device, a method for performing operations for rotation and/or scaling of polygon-based 3D graphic objects to be displayed on the display device, comprising the steps of:

computing display screen position coordinates for a rotated and/or scaled polygon-based object; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object to the video RAM.

187. (Previously Presented) A home video game system for use with a television type monitor display device, said system contained at least in part in a housing having an insertion port for receiving a removable memory storage device storing video game program instructions and/or data, comprising:

a game program processor;

a graphics processor for rendering at least one or more portioning of a polygon-based 3D graphic object for displaying on the display device; and

a CD ROM reader device, wherein at least a portion of program instructions and/or graphics data used in rendering a 3D graphic object is accessed from a CD ROM.

188. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

189. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor is a pipelined processor.

190. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor includes a high speed multiplier circuit.

191. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor includes a plurality of data storage registers.

192. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor includes geometry transformation circuitry for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

193. (Previously Presented) A home video game system as in claim 192 wherein the geometry transformation circuitry includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

194. (Previously Presented) A home video game system as set forth in claim 193 wherein the multiplier circuit performs multiply operations using at least 16-bit length operands.

195. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

196. (Previously Presented) A home video game system as in claim 187 wherein two or more polygon-based 3D graphic objects are displayed simultaneously.

197. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor is programmed to perform texture mapping operations.

198. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

199. (Previously Presented) A home video game system as in claim 187 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

200. (Previously Presented) A home video game system as in claim 187 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

201. (Previously Presented) A home video game system as in claim 187 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

202. (Previously Presented) In a home video game system having an insertion port for receiving removable memory for storing video game program data and/or instructions, said system including a game program processor and a programmable pipelined graphics processor, a method for performing operations for rotation and/or scaling of polygon-based 3D graphic objects to be displayed on a raster scan type display device, comprising the steps of:

computing bit mapped display screen position object coordinates for a rotated and/or scaled polygon-based ~~an~~ object to be displayed; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object to a video display RAM.

203. (Previously Presented) The method as in claim 202 wherein the writing of pixel information is accomplished via a direct memory access (DMA) operation.

204. (Previously Presented) In a home video game system, having a game program processor and a programmable graphics processor, the graphics processor having circuitry for increasing computational speed when processing 3D graphic geometric transformation operations, a method of producing 3D type graphics display effects utilizing rotated and/or scaled polygon-based objects, comprising the steps of:

providing said graphics processor with information relating at least in part to a polygon based graphic object; and

writing pixel color information corresponding to the rotated and/or scaled polygon-based object a video display RAM.

205. (Previously Presented) The method as in claim 204 wherein the writing of pixel information is accomplished via a DMA operation.

206. (Previously Presented) A home video game system for use with a television type monitor display device, said system contained, at least in part, in a housing defining an insertion space for receiving a portable removable non-volatile memory storing instructions and data relating to one or more polygon-based 3D graphic objects, comprising:

a programmable graphics processor; and

a main processor that accesses said instructions and data and communicates information relating to one or more polygon-based 3D graphic objects to the programmable graphics processor,

wherein the programmable graphics processor is programmed to render at least one or more portions of said polygon-based 3D graphic objects for displaying on said display device.

207. (Previously Presented) A home video game system as in claim 206 wherein the programmable graphics processor is a coprocessor that is responsive to specific instructions used for rendering 3D objects.

208. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor is a pipelined processor.

209. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor is a programmable pipelined processor.

210. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor includes embedded RAM cache memory.

211. (Previously Presented) A home video game system as in claim 206 wherein the programmable graphics processor includes a high speed multiplier for performing computations for performing rotation and/or scaling of a 3D graphic object or portions of the object to be displayed.

212. (Previously Presented) A home video game system as in claim 206 wherein the programmable graphics processor includes at least an Arithmetic Logic Unit and a multiplier circuit for performing computations for rotation and/or scaling of a polygon-based graphic object to be displayed.

213. (Previously Presented) A home video game system as set forth in claim 212 wherein the multiplier performs multiply operations using at least 16-bit length operands.

214. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor is programmed to rotate an array of data corresponding to polygon vertex points.

215. (Previously Presented) A home video game system as in claim 206 wherein two or more polygon-based graphic objects are displayed simultaneously.

216. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor is programmed to perform texture mapping operations.

217. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor includes a pixel plotting circuit for converting display screen pixel coordinate addresses to a character map address format.

218. (Previously Presented) A home video game system as in claim 206 having a set of instructions for programming the graphics processor unit for rendering 3D objects wherein the instruction set includes an instruction for controlling transparency of a displayed object.

219. (Previously Presented) A home video game system as in claim 206 having a set of instructions for programming the graphics processor unit wherein the instruction set includes a fractional signed multiply instruction for computing gradients and/or slopes for rotating polygon-based displayed objects.

220. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and cache RAM fabricated on a single chip.

221. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor incorporates at least an Arithmetic Logic Unit and a high speed multiplier circuit fabricated on a single chip.

222. (Previously Presented) A home video game system as in claim 206 wherein the graphics processor comprises an Arithmetic Logic Unit, a multiplier unit and plurality of registers fabricated on a single chip.

223. (Previously Presented) A home video game system as in claim 206 further comprising a CD ROM reader device wherein at least a portion of program instructions and/or graphics data is accessed from a CD ROM.